
HZX-52832-S01A Bluetooth 4.0

Low Energy Module

Datasheet

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2017.4

NAME : Bluetooth 4.0 Low Energy Module

MODEL NO. : HZX-52832-S01A

VERSION : V1.0

1.Revision History

Revision	Description	Approved	Date
V1.0	Initial Release	Kevin	2017.4

CONTENTS

1. Revision History.....	1
2. Product Description.....	3
3. Key Features.....	4
4. Applications.....	6
5. Application Block Diagram.....	7
6. Interfaces.....	8
6.1 Power Supply.....	8
6.2 System Function Interfaces.....	8
6.2.1 GPIOs.....	8
6.2.2 Two-wire Interface (I ₂ C Compatible).....	9
6.2.3 Flash Program I/Os.....	9
6.2.4 Serial Peripheral Interface.....	9
6.2.5 UARTs	10
6.2.6 Analog to Digital Converter (ADC)	11
6.2.7 Low Power Comparator (LPCOMP)	11
6.2.8 Reset	12
6.2.9 NFC	12
7. Module Pinout and Pin Description.....	13
7.1 Module Pinout	13
7.2 Pin Description	14
8. PCB Design Guide.....	15
9. PCB Footprint and Dimensions.....	16
10. Electrical Characteristics.....	17
11. Manufacturing Process Recommendations.....	18
12. Contact Information.....	19

2. Product Description

The HZX-52832-S01A is a highly integrated Bluetooth 4.0 BLE module with NFC function, it was designed for high data rate, short-range wireless communication in the 2.4GHz ISM band. The module is designed based on Nordic Semiconductor nRF52832 radio Transceiver IC, has a 32 bit ARM Cortex-M4 CPU, flash memory and analog and digital peripherals. The HZX-52832-S01A provides a low power and ultra-low cost BLE and proprietary protocols for wireless transmission applications.

The HZX-52832-S01A is a 13.8mm×21mm micro-module with embedded PCB antenna. It allows developers to take full advantage of the nRF52832 by making all its I/O available via 34 SMD/Through hole 1.2mm pitch pads. The module can be mounted with header pins in order to re-use during development and prototyping phase and SMD it for production to be the most cost effective.

Figure 1: HZX-52832-S01A Top View

3.ey Features

- ◆ 32 bits ARM® Cortex™-M4 @ 16MHz
- ◆ 2.4GHz multi-protocol transceiver
- ◆ 64KB SRAM
- ◆ 512KB Flash
- ◆ 32 configurable I/O pins, 19 General Purpose I/O pins
- ◆ One 32 and two 16 bit timers with counter mode
- ◆ 20 channel CPU independent Programmable Peripheral Interconnect (PPI)
- ◆ Encryption - 128 bit AES ECB/CCM/AAR co-processor
- ◆ RNG, RTC
- ◆ Temperature sensor
- ◆ Digital interfaces SPI Master/Slave, 2-wire Master (I2C compatible), UART (CTS/RTS), IIS, PDM
- ◆ Quadrature decoder
- ◆ 12bit 200KSPS ADC - 8 configurable channels
- ◆ Low power comparator
- ◆ -96dBm sensitivity
- ◆ Single-ended antenna

- ◆ NFC-A tag
- ◆ Tx Power -20 to +4 dBm in 4 dB steps
- ◆ 7.5mA TX at +4dBm
- ◆ Operating voltage : 1.7V to 3.6V
- ◆ Dimension : 13.8mm×21mm

4. Applications

- ◆ Computer peripherals and I/O devices

- Mouse

- Keyboard

- Multi-touch trackpad

- ◆ Interactive entertainment devices

- Remote control

- 3D Glasses

- Gaming controller

- ◆ Personal Area Networks

- Health/fitness sensor and monitor devices

- Medical devices

- Key-fobs + wrist watches

- ◆ Remote control toys

- ◆ Beacons

- ◆ Bluetooth Gateway

- ◆ Indoor Location

5.Application Block Diagram

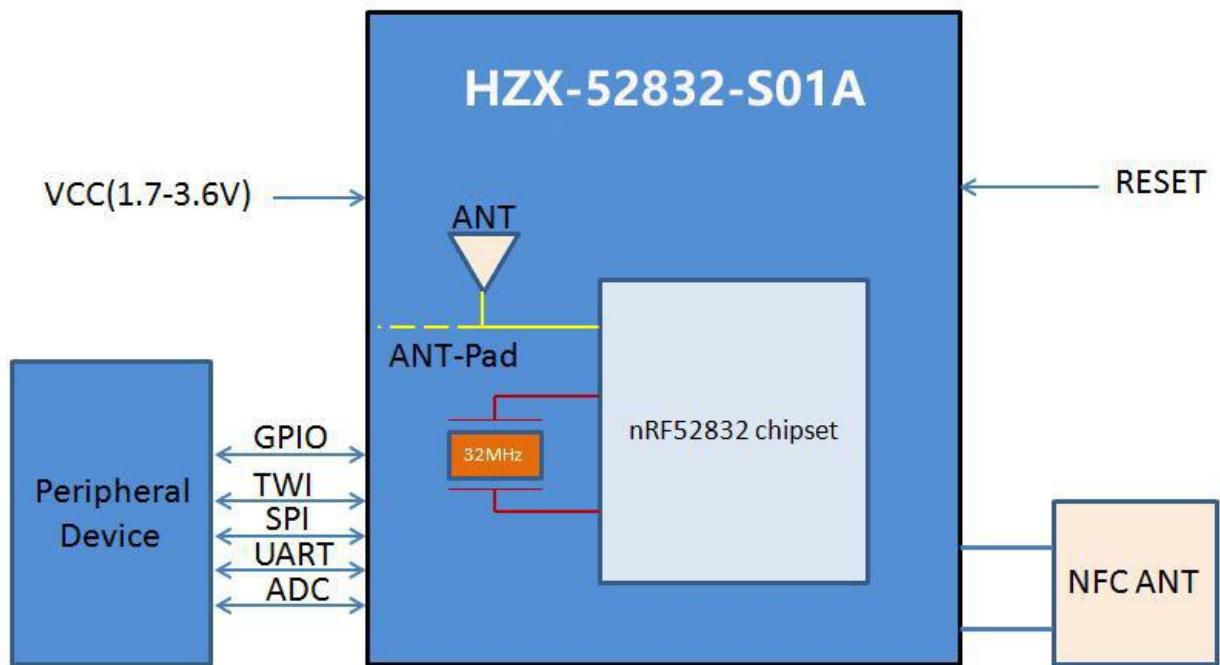


Figure 2: HZX-52832-S01A Block Diagram

6.Interfaces

6.1 Power Supply

Regulated power for the HZX-52832-S01A is required. The input voltage Vcc range should be 1.7V to 3.6V. Suitable decoupling must be provided by external decoupling circuitry (10uF and 0.1uF). It can reduce the noise from power supply and increase power stability.

6.2 System Function Interfaces

6.2.1 GPIOs

The general purpose I/O is organized as one port with up to 19 I/Os enabling access and control of up to 19 pins through one port. Each GPIO can be accessed individually with the following user configurable features:

- ◆ Input/output direction
- ◆ Output drive strength
- ◆ Internal pull-up and pull-down resistors
- ◆ Wake-up from high or low level triggers on all pins
- ◆ Trigger interrupt on all pins
- ◆ All pins can be used by the PPI task/event system; the maximum number of pins that can be interfaced through the PPI at the same time is limited by the number of GPIOTE channels
- ◆ All pins can be individually configured to carry serial interface or quadrature demodulator signals

- ◆ All pins can be configured as PWM signal
- ◆ There are 6 ADC/LPCOMP input in the 19 I/Os

6.2.2 Two-wire Interface (I2C Compatible)

The two-wire interface can communicate with a bi-directional wired-AND bus with two lines (SCL, SDA). The protocol makes it possible to interconnect up to 127 individually addressable devices. The interface is capable of clock stretching, supporting data rates of 100 kbps ,250kbps and 400 kbps. The module has 2 TWI ports and they properties like following table.

Instance	Master/Slave
TWI 0	Master
TWI 1	Master

Table 1: TWI Pins share scheme

Note: I2C:Inter—Integrated Circuit

6.2.3 Flash Program I/Os

The module has two programmer pins, respectively SWDCLK pin and SWDIO pin. The two pin Serial Wire Debug (SWD) interface provided as a part of the Debug Access Port (DAP) offers a flexible and powerful mechanism for non-intrusive debugging of program code. Breakpoints and single stepping are part of this support.

6.2.4 Serial Peripheral Interface

The SPI interfaces enable full duplex synchronous communication between devices. They support a three-wire (SCK, MISO, MOSI) bi-directional bus with

fast data transfers. The SPI Master can communicate with multiple slaves using individual chip select signals for each of the slave devices attached to a bus. Control of chip select signals is left to the application through use of GPIO signals. SPI Master has double buffered I/O data. The SPI Slave includes EasyDMA for data transfer directly to and from RAM allowing Slave data transfers to occur while the CPU is IDLE. The GPIOs are used for each SPI interface line can be chosen from any GPIOs on the device and independently. This enables great flexibility in device pinout and efficient use of printed circuit board space and signal routing.

The SPI peripheral support SPI mode 0,1,2, and 3. The module have 3 SPI ports and theirs properties are as below:

Instance	Master/Slave
SPI 0	Master
SPI 1	Master
SPIS 1	Slave

Table 2: SPI Properties

6.2.5 UARTs

The Universal Asynchronous Receiver/Transmitter offers fast, full-duplex, asynchronous serial communication with built-in flow control (CTS, RTS), support in hardware up to 1 Mbps baud. Parity checking is supported.

Support the following baudrate in bps unit:

1200/2400/4800/9600/14400/19200/28800/38400/57600/76800/115200.

Note: The GPIOs are used for each SPI/TWI/UART interface line can be chosen from any GPIOs on the device and configed independently.

6.2.6 Analog to Digital Converter (ADC)

The 12 bit incremental Analog to Digital Converter (ADC) enables sampling of up to 8 external signals through a front-end multiplexer. The ADC has configurable input and reference prescaling, and sample resolution (8,10, and 12 bit).

Note: The ADC module uses the same analog inputs as the LPCOMP module. Only one of the modules can be enabled at the same time.

HZX-52832-S01A Pin Number	Pin Number	Description
4	P0.28	Digital I/O; Analog input 4
5	P0.29	Digital I/O; Analog input 5
6	P0.30	Digital I/O; Analog input 6
7	P0.31	Digital I/O; Analog input 7
8	P0.02	Digital I/O; Analog input 0
11	P0.03	Digital I/O; Analog input 1
12	P0.04	Digital I/O; Analog input 2
13	P0.05	Digital I/O; Analog input 3

Table 3: ADC Pins

6.2.7 Low Power Comparator (LPCOMP)

In System ON, the block can generate separate events on rising and falling edges of a signal, or sample the current state of the pin as being above or below the threshold. The block can be configured to use any of the analog inputs on the device. Additionally, the low power comparator can be used as an analog wakeup source from System OFF or System ON. The comparator threshold can be programmed to a range of fractions of the supply voltage.

6.2.8 Reset

The reset pin of the HZX-52832-S01A module is in the internal pull-high state , when the reset pin of the module is input to a low level , the module will be automatically reset .After the reset pin is used , the parameters of the current setting will not be reserved .

6.2.9 NFC

The NFC peripheral (referred to as the 'NFC peripheral' from now on) supports communication signal interface type A and 106 kbps bit rate from the NFC Forum.

With appropriate software, the NFC peripheral can be used to emulate the listening device NFC-A as specified by the NFC Forum.

Listed here are the main features for the NFC peripheral:

- ◆ NFC-A listen mode operation
- ◆ 13.56 MHz input frequency
- ◆ Bit rate 106 kbps
- ◆ Wake-on-field low power field detection (SENSE) mode
- ◆ Frame assemble and disassemble for the NFC-A frames specified by the NFC Forum
- ◆ Programmable frame timing controller
- ◆ Integrated automatic collision resolution, CRC and parity functions

HZX-52832-S01A Pin Number	Pin Number	Description
17	P0.09	Digital I/O; NFC1
18	P0.10	Digital I/O; NFC2

Table 4: NFC Pins

7. Module Pinout and Pin Description

7.1 Module Pinout

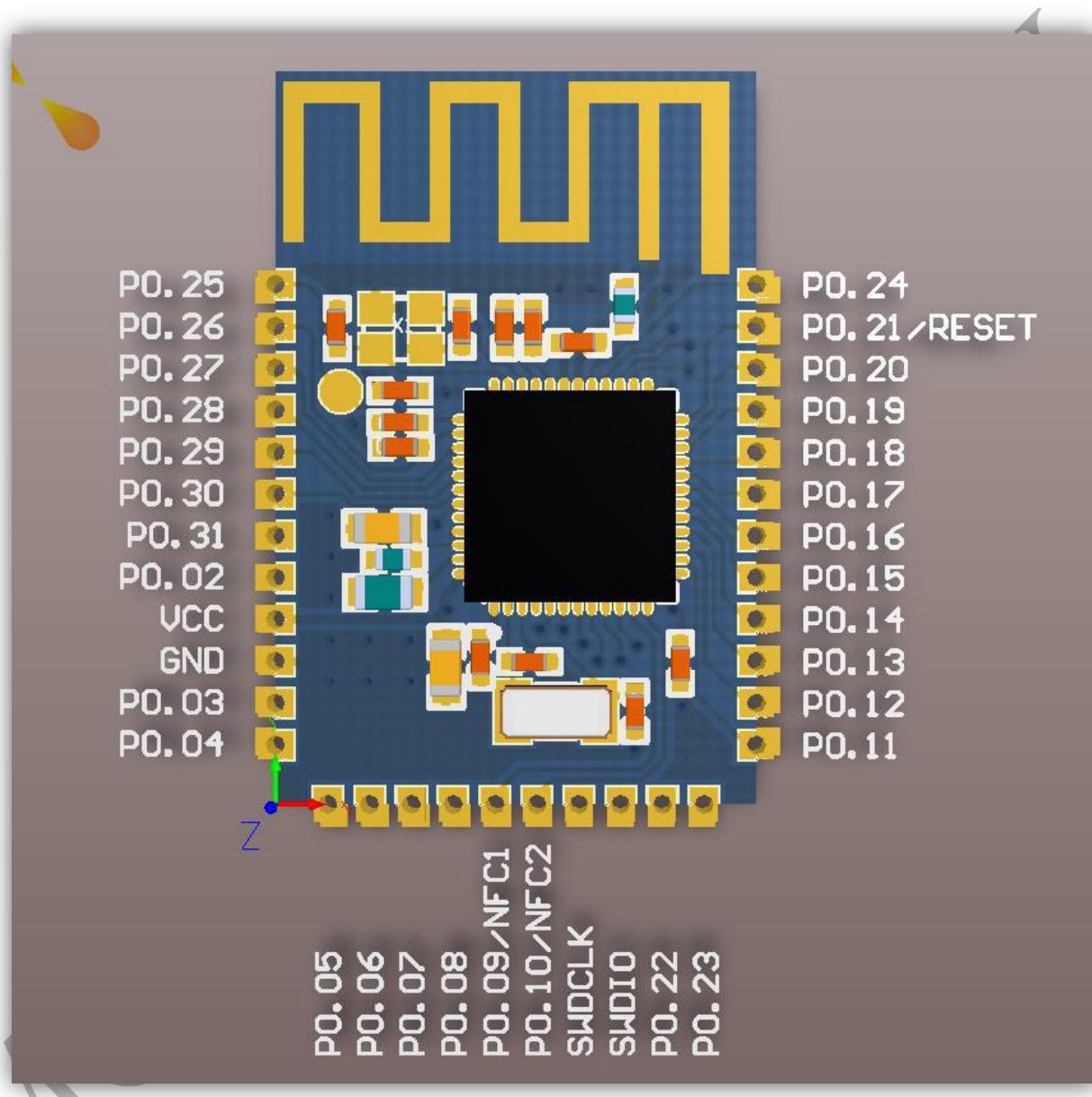


Figure 3: HZX-52832-S01A Module Pinout

7.2 Pin Description

Pin NO.	Pin Name	Description	Remark
1	P0.25	General Purpose I/O	Digital I/O
2	P0.26	General Purpose I/O	Digital I/O
3	P0.27	General Purpose I/O	Digital I/O
4	P0.28	Digital I/O; Analog input 4	SAADC/COMP/LPCOMP input
5	P0.29	Digital I/O; Analog input 5	SAADC/COMP/LPCOMP input
6	P0.30	Digital I/O; Analog input 6	SAADC/COMP/LPCOMP input
7	P0.31	Digital I/O; Analog input 7	SAADC/COMP/LPCOMP input
8	P0.02	Digital I/O; Analog input 0	SAADC/COMP/LPCOMP input
9	VCC	Power Supply	1.7V-3.6V
10	GND	Ground	
11	P0.03	Digital I/O; Analog input 1	SAADC/COMP/LPCOMP input
12	P0.04	Digital I/O; Analog input 2	SAADC/COMP/LPCOMP input
13	P0.05	Digital I/O; Analog input 3	SAADC/COMP/LPCOMP input
14	P0.06	General Purpose I/O; TX	Digital I/O
15	P0.07	General Purpose I/O; RX	Digital I/O
16	P0.08	General Purpose I/O	Digital I/O
17	P0.09/NFC1	General Purpose I/O; NFC1	Digital I/O
18	P0.10/NFC2	General Purpose I/O; NFC2	Digital I/O
19	SWDCLK	Digital input	Hardware Debug and Flash Program I/O
20	SWDIO	Digital I/O	
21	P0.22	General Purpose I/O	Digital I/O
22	P0.23	General Purpose I/O	Digital I/O
23	P0.11	General Purpose I/O	Digital I/O
24	P0.12	General Purpose I/O	Digital I/O
25	P0.13	General Purpose I/O	Digital I/O
26	P0.14	General Purpose I/O	Digital I/O
27	P0.15	General Purpose I/O	Digital I/O
28	P0.16	General Purpose I/O	Digital I/O
29	P0.17	General Purpose I/O	Digital I/O
30	P0.18	General Purpose I/O	Digital I/O
31	P0.19	General Purpose I/O	Digital I/O
32	P0.20	General Purpose I/O	Digital I/O
33	P0.21/RESET	General Purpose I/O; nRESET	Digital I/O
34	P0.24	General Purpose I/O	Digital I/O

8. PCB Design Guide

Please reserve empty area for PCB antenna when you are going to design a device's board, the empty range minimum size : $13.8 \times 5.4\text{mm}$, please kindly check the Figure 5 below for reference.

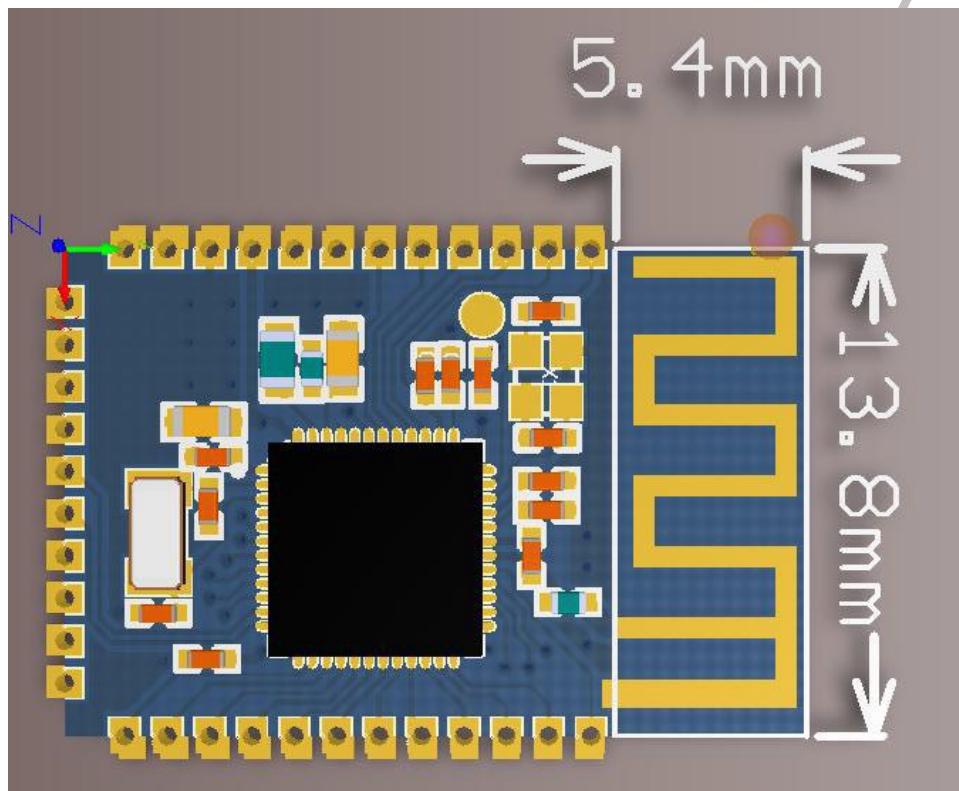


Figure 4: HZX-52832-S01A PCB Antenna Size

9. PCB Footprint and Dimensions

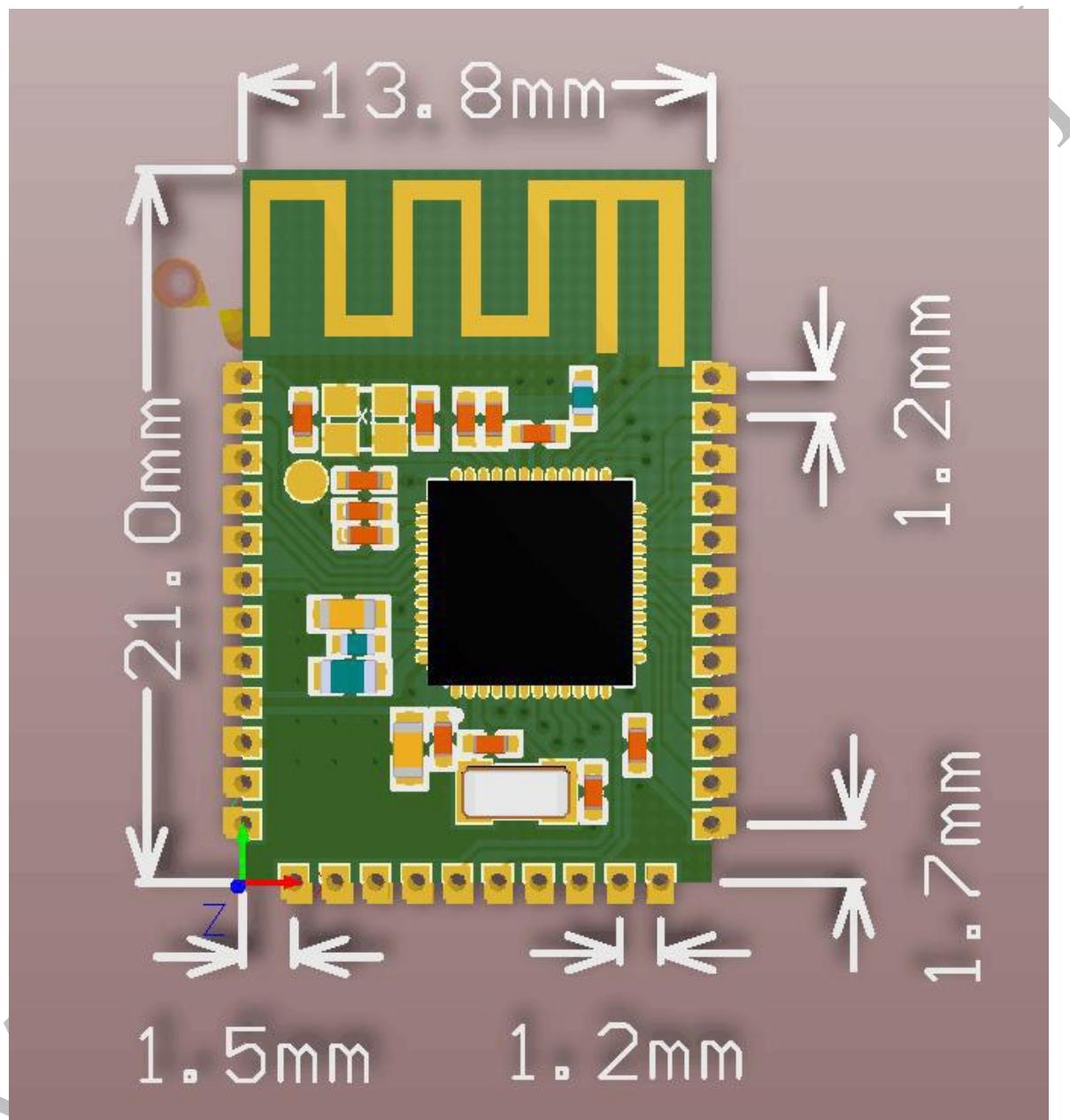


Figure 5: HZX-52832-S01A PCB Footprint and Dimensions

10. Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
Extended Temp. Range	TA	-40	25	85	°C
Power Supply	VCC	1.7	3.3	3.6	V
Input Low Voltage	VIL	0	/	$0.3 \times VCC$	V
Input High Voltage	VIH	$0.7 \times VCC$	/	VCC	V

Table 5: Operating Conditions

11. Manufacturing Process Recommendations

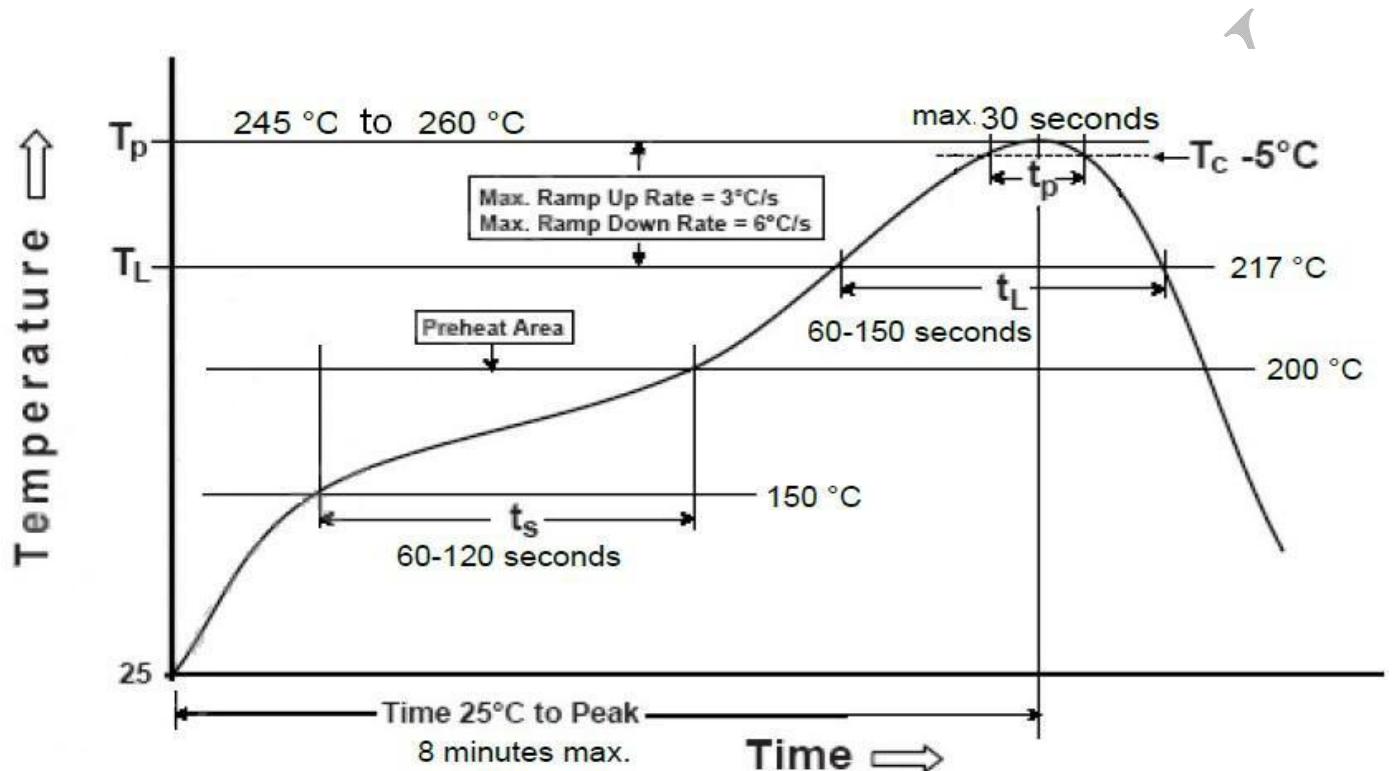


Figure 6: HZX-52832-S01A Typical Lead-free Soldering Profile

Note: The final re-flow soldering temperature map chosen at the factory depends on additional external factors, for example, choice of soldering paste, size, thickness and properties of the module's baseboard etc. Exceeding the maximum soldering temperature in the recommended soldering profile may permanently damage the module.

12. Contact Information

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