HZX-51822-16M04 Bluetooth 4.0 Low Energy Module Datasheet

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2017.7

NAME : Bluetooth 4.0 Low Energy Module

MODEL NO. : HZX-51822-16M04

VERSION : V1.0

1.Revision History

Revision	Description	Approved	Date
V1.0	Initial Release	Kevin	2017.7

CONTENTS

2.Product Description

The HZX-51822-16M04 is a highly integrated Bluetooth 4.0 BLE module. The module is designed based on Nordic Semiconductor nRF51822 radio Transceiver IC-- the Multiprotocol Bluetooth® 4.0 low energy/2.4 GHz RF SoC designed for ULP (ultra low power) wireless, has a 32 bit ARM Cortex-M0 CPU, flash memory and analog and digital peripherals. The HZX-51822-16M04 provides a low power and ultra-low cost BLE and proprietary protocols for wireless transmission applications.

The HZX-51822-16M04 is a 17mm×25mm micro-module with embedded PCB antenna. It allows developers to take full advantage of the nRF51822 by making all its I/O (except P0.26 and P0.27 for 32.768 kHz crystal oscillator)available via 36 SMD/Through hole 1.1mm pitch pads. The module can be mounted with header pins in order to re-use during development and prototyping phase and SMD it for production to be the most cost effective.

You can chose the module HZX-51822-16M04G, which has an ultra-low-power high performance three-axis linear accelerometer device(G-sensor)—LIS3DH.

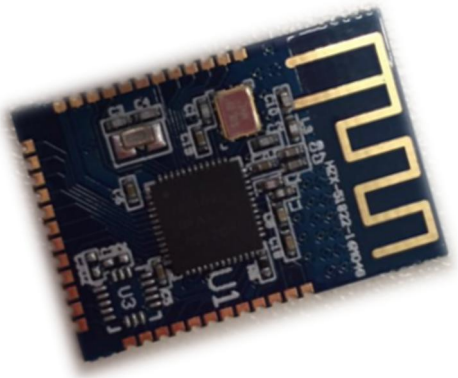

Fig 1: HZX-51822-16M04 Top View (without shield cover)

3.Specifications & Features

◆Onboard chip: nRF51822qfaa (you can use nRF51822qfac instead if necessary)

◆Communication distance (open outdoor@1M data rate): 30m

◆Frequency range: 2.4GHz

◆256kB flash & 16kB RAM(nRF51822qfaa) or 32kB RAM(nRF51822qfac)

◆Operating voltage: 2.0V ~ 3.6V(Internal LDO) or 1.8V~3.6V(External LDO)

◆Operating temperature: -40℃ ~ 85℃

◆Programmable output power: -20 to +4 dBm

◆Expansion pinheader: all the I/Os except P0.26 and P0.27 (used for 32.768 kHz crystal oscillator)

◆Digital interfaces: SPI Master/Slave, I2C, UART(CTS/RTS)

◆CPU independent programmable Peripheral Interconnect(PPI)

◆Fully compatible with NRF24L series

◆8/9/10bit ADC- configurable

◆S100 series SoftDevice ready

◆Quadrature Decoder (QDEC)

◆AES HW encryption

◆Real Timer Counter (RTC)

◆Antenna: onboard antenna

◆Ultra-low-power high performance three-axis linear accelerometer device (Only HZX-51822-16M04G)

4.Applications

◆Computer peripherals and I/O devices
Mouse
Keyboard
Multi-touch trackpad

◆Interactive entertainment devices
Remote control
3D Glasses
Gaming controller

◆Personal Area Networks
Health/fitness sensor and monitor devices
Medical devices
Key-fobs + wrist watches

◆Remote control toys

◆Beacons

◆Bluetooth Gateway

◆Indoor Location

5.Application Block Diagram

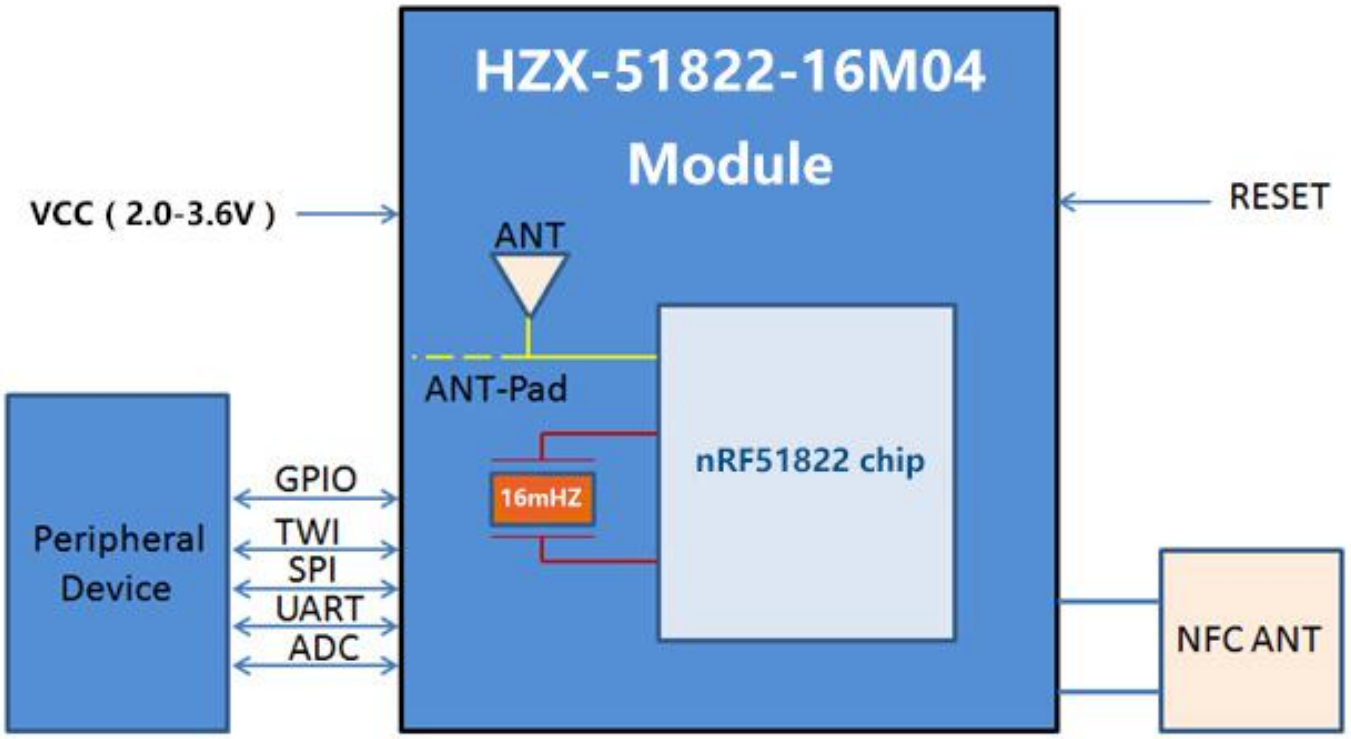

Figure 2: HZX-51822-16M04 Block Diagram

6.Interfaces

6.1 Power Supply

Regulated power for the HZX-51822-16M04 is required. The input voltage VCC range should be 1.8V to 3.6V (External LDO) or 2.0V to 3.6V (Internal LDO). Suitable decoupling must be provided by external decoupling circuitry (10uF and 0.1uF). It can reduce the noise from power supply and increase power stability.

6.2 System Function Interfaces

6.2.1 GPIOs

The general purpose I/O is organized as one port with up to 29 I/Os enabling access and control of up to 29 pins through one port. Each GPIO can be accessed individually with the following user configurable features:

◆Input/output direction

◆Output drive strength

◆Internal pull-up and pull-down resistors

◆Wake-up from high or low level triggers on all pins

◆Trigger interrupt on all pins

◆All pins can be used by the PPI task/event system; the maximum number of pins that can be interfaced through the PPI at the same time is limited by the number of GPIOTE channels

◆All pins can be individually configured to carry serial interface or quadrature demodulator signals

◆There are 7 ADC/LPCOMP input in the 29 I/Os

6.2.2 Two-wire Interface (TWI/I2C Compatible)

The two-wire interface can communicate with a bi-directional wired-AND bus with two lines (SCL, SDA). The protocol makes it possible to interconnect up to 127 individually addressable devices. The interface is capable of clock stretching, supporting data rates of 100 kbps and 400 kbps.

The GPIOs used for each two-wire interface line can be chosen from any GPIO on the device and are independently configurable. This enables great flexibility in device pinout and efficient use of board space and signal routing.

Instance	Master/Slave
TWI 0	Master
TWI 1	Master

Table 1: TWI Pins share scheme

6.2.3 Flash Program I/Os

The module has two programmer pins, respectively SWDCLK pin (P29) and SWDIO pin (P28). The two pin Serial Wire Debug (SWD) interface provided as a part of the Debug Access Port (DAP) offers a flexible and powerful mechanism for non-intrusive debugging of program code. Breakpoints and single stepping are part of this support.

6.2.4 Serial Peripheral Interface

The SPI interfaces enable full duplex synchronous communication between devices. They support a three-wire (SCK, MISO, MOSI) bi-directional bus with fast data transfers. The SPI Master can communicate with multiple slaves using individual chip select signals for each of the slave devices attached to a bus. Control of chip select signals is left to the application through use of GPIO signals. SPI Master has double buffered I/O data. The SPI Slave includes

EasyDMA for data transfer directly to and from RAM allowing Slave data transfers to occur while the CPU is IDLE.

The GPIOs used for each SPI interface line can be chosen from any GPIO on the device and are independently configurable. This enables great flexibility in device pinout and efficient use of printed circuit board space and signal routing.

The SPI peripheral support SPI mode 0, 1, 2, and 3.

Instance	Master/Slave
SPI 0	Master
SPI 1	Master
SPIS 1	Slave

Table 2: SPI Properties

6.2.5 Universal Asynchronous Receiver/Transmitter (UART)

The Universal Asynchronous Receiver/Transmitter offers fast, full-duplex, asynchronous serial communication with built-in flow control (CTS, RTS) support in hardware up to 1 Mbps baud. Parity checking is supported.

The GPIOs used for each UART interface line can be chosen from any GPIO on the device and are independently configurable. This enables great flexibility in device pinout and efficient use of board space and signal routing.

6.2.6 Analog to Digital Converter (ADC)

The 10 bit incremental Analog to Digital Converter (ADC) enables sampling of up to 8 external signals through a front-end multiplexer. The ADC has configurable input, reference prescaling, and sample resolution (8, 9, and 10 bit).

Note: The ADC module uses the same analog inputs as the LPCOMP module. Only one of the modules can be enabled at the same time.

HZX-51822-16M04 Pin Number	Pin Number	Description
14	P0.00	Digital I/O; Analog input 0
15	P0.01	Digital I/O; Analog input 2
16	P0.02	Digital I/O; Analog input 3
17	P0.03	Digital I/O; Analog input 4
18	P0.04	Digital I/O; Analog input 5
19	P0.05	Digital I/O; Analog input 6
20	P0.06	Digital I/O; Analog input 7

Table 3: ADC Pins

6.2.7 Low Power Comparator (LPCOMP)

In System ON, the block can generate separate events on rising and falling edges of a signal, or sample the current state of the pin as being above or below the threshold. The block can be configured to use any of the analog inputs on the device. Additionally, the low power comparator can be used as an analog wakeup source from System OFF or System ON. The comparator threshold can be programmed to a range of fractions of the supply voltage.

Note: The LPCOMP module uses the same analog inputs as the ADC module. Only one of the modules can be enabled at the same time.

6.2.8 Reset

The reset pin of the HZX-51822-16M04 module is in the internal pull-high state , when the reset pin of the module is input to a low level , the module will be automatically reset .After the reset pin is used , the parameters of the current setting will not be reserved .

7. Module Pinout and Pin Description

7.1 Module Pinout

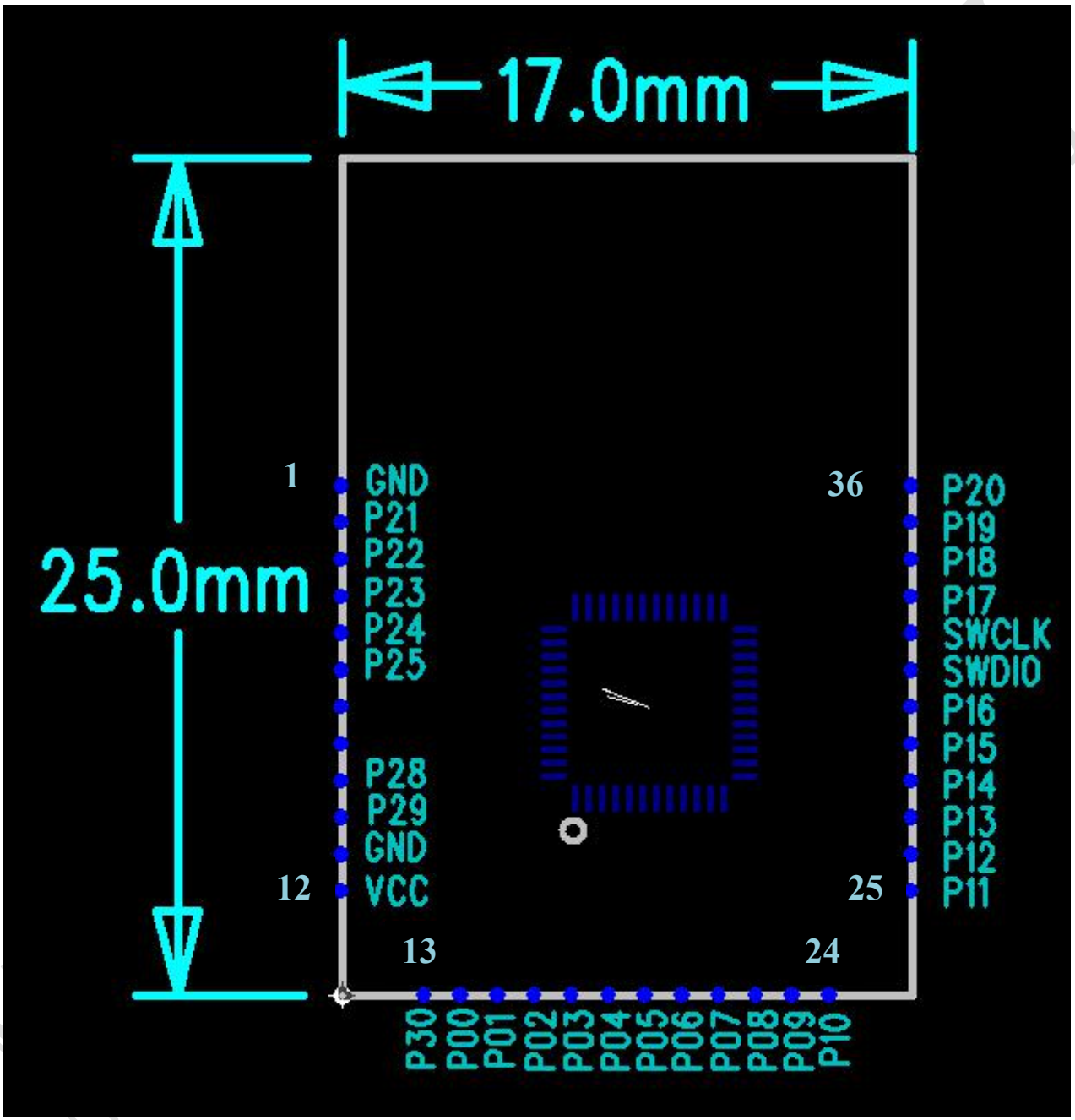

Figure 3: HZX-51822-16M04 Module Pinout

7.2 Pin Description

Pin NO.	Pin Name	Description	Remark
1	GND	Ground	Ground
2	P0.21	General Purpose I/O	Digital I/O
3	P0.22	General Purpose I/O	Digital I/O
4	P0.23	General Purpose I/O	Digital I/O
5	P0.24	General Purpose I/O	Digital I/O
6	P0.25	General Purpose I/O	Digital I/O
7	NC	NC	
8	NC	NC	
9	P0.28	General Purpose I/O	Digital I/O
10	P0.29	General Purpose I/O	Digital I/O
11	GND	Ground	Ground
12	VCC	Power Supply	2.0V-3.6V
13	P0.30	General Purpose I/O	Digital I/O
14	P0.00	Digital I/O; Analog input 0	SAADC/COMP/LPCOMP input
15	P0.01	Digital I/O; Analog input 2	SAADC/COMP/LPCOMP input
16	P0.02	Digital I/O; Analog input 3	SAADC/COMP/LPCOMP input
17	P0.03	Digital I/O; Analog input 4	SAADC/COMP/LPCOMP input

18	P0.04	Digital I/O; Analog input 5	SAADC/COMP/LPCOMP input
19	P0.05	Digital I/O; Analog input 6	SAADC/COMP/LPCOMP input
20	P0.06	Digital I/O; Analog input 7	SAADC/COMP/LPCOMP input
21	P0.07	General Purpose I/O	Digital I/O
22	P0.08	General Purpose I/O	Digital I/O
23	P0.09	General Purpose I/O; RX	Digital I/O
24	P0.10	General Purpose I/O	Digital I/O
25	P0.11	General Purpose I/O; TX	Digital I/O
26	P0.12	General Purpose I/O	Digital I/O
27	P0.13	General Purpose I/O	Digital I/O
28	P0.14	General Purpose I/O	Digital I/O
29	P0.15	General Purpose I/O	Digital I/O
30	P0.16	General Purpose I/O	Digital I/O
31	SWDIO	Digital I/O; nRESET	System reset (active low). Hardware debug and flash programming I/O
32	SWDCLK	Digital input	Hardware debug and flash programming I/O
33	P0.17	General Purpose I/O	Digital I/O
34	P0.18	General Purpose I/O	Digital I/O
35	P0.19	General Purpose I/O	Digital I/O
36	P0.20	General Purpose I/O	Digital I/O

8. PCB Design Guide

Please reserve empty area for PCB antenna when you are going to design a device's board, please kindly check the Figure 4 below for reference.

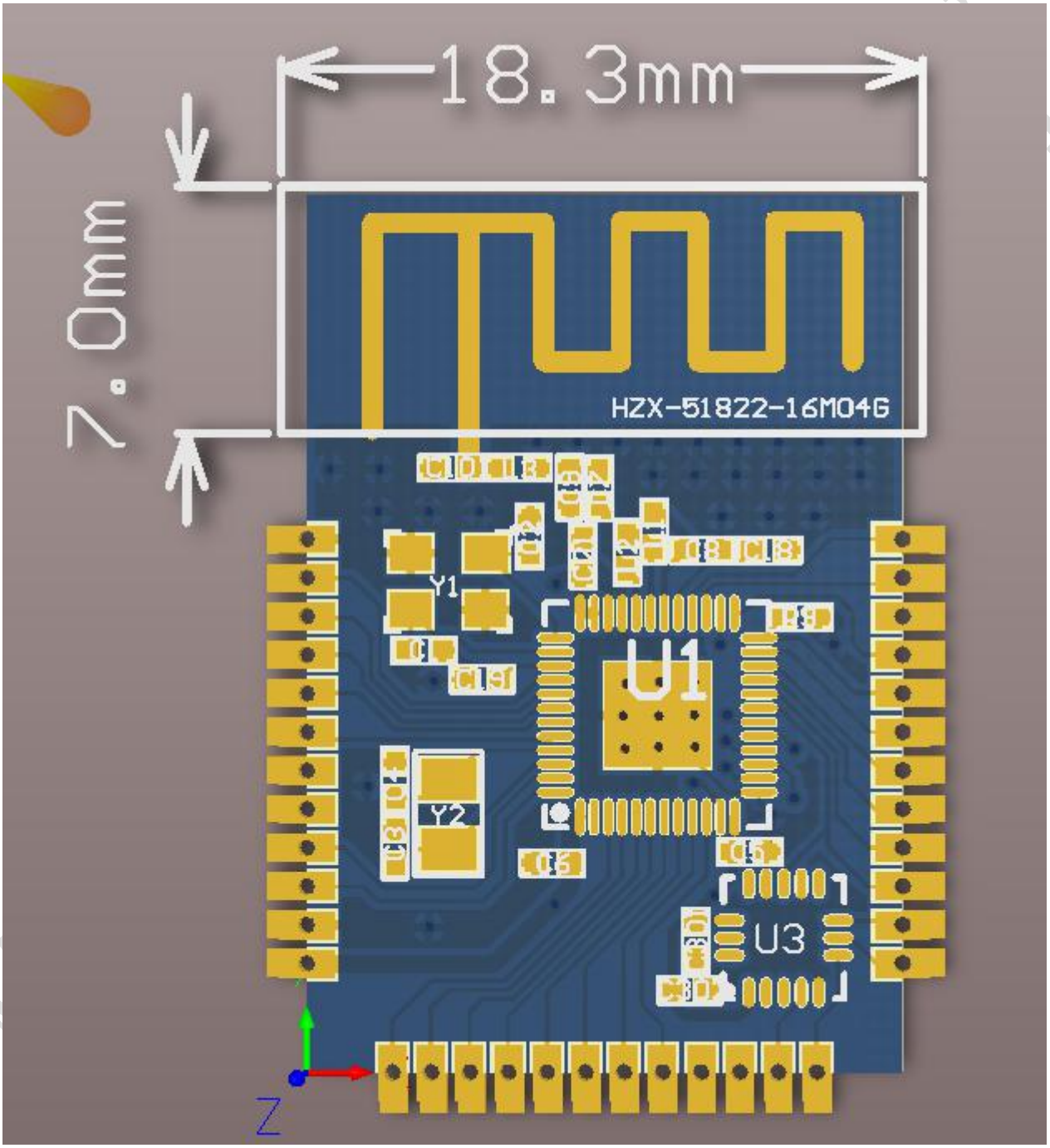

Figure 4: HZX-51822-S04 PCB Antenna

9. PCB Footprint and Dimensions

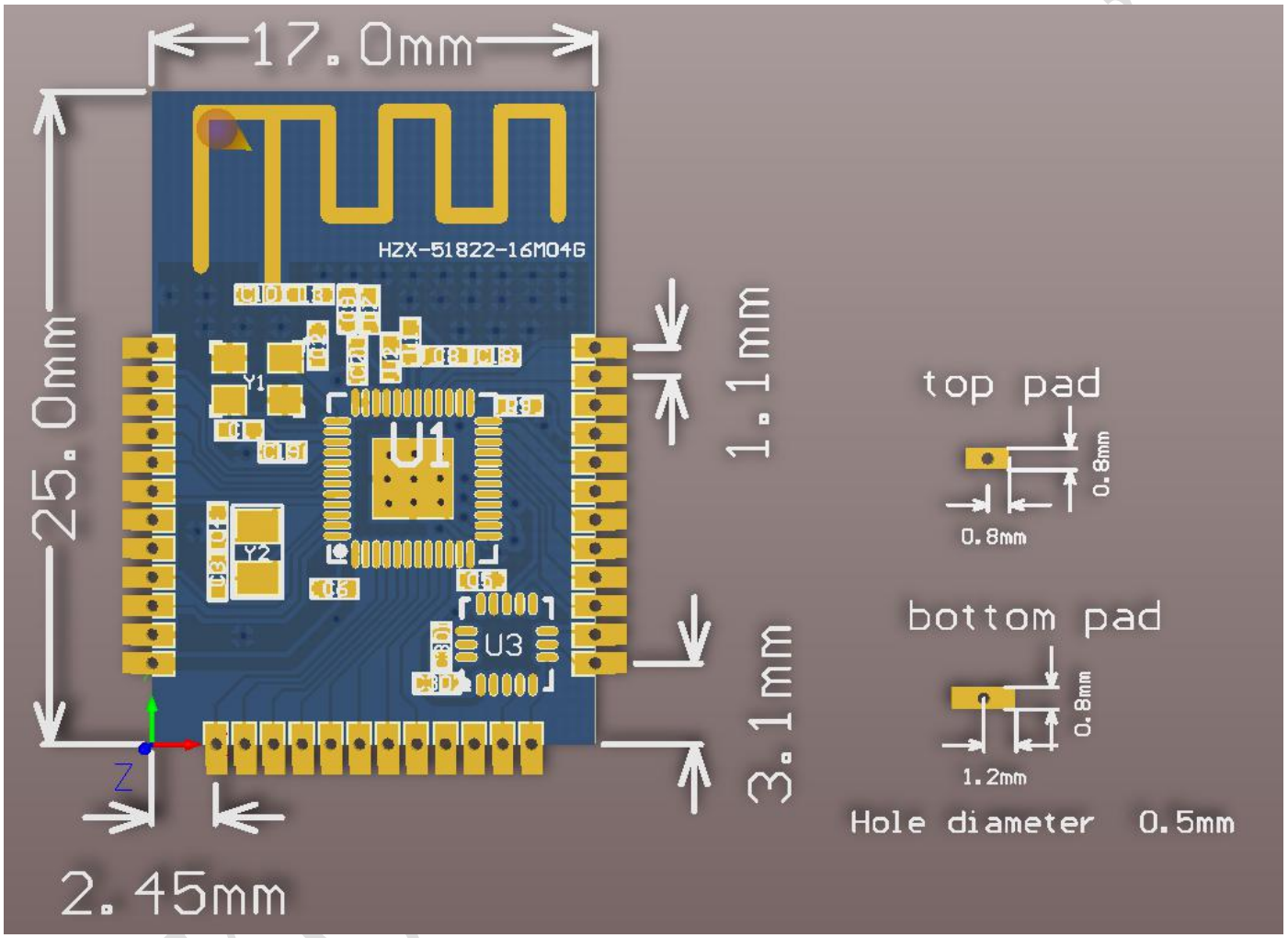

Figure 5: HZX-51822-S04 PCB Footprint and Dimensions

10. Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Extended Temp. Range	TA	-40	25	85	ºC
Power Supply	VCC	2.0	3.3	3.6	V
Input Low Voltage	VIL	0	/	0.3*VCC	V
Input High Voltage	VIH	0.7*VCC	/	VCC	V

Table 4: Operating Conditions

11. Contact Information

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